



ELECTRONIC ENGINEERING

DECEMBER 5, 2005

EE TIMES

The industry newsweekly for the creators of technology

Great Minds, Great Ideas

A SUPPLEMENT TO EE TIMES

THE PEOPLE, PRODUCTS AND TECHNOLOGIES THAT ARE
CHANGING THE WAY WE LIVE, WORK AND PLAY

SPECIAL COLLECTOR'S EDITION

In his spare time, Zvi Or-Bach loves Israeli folk dancing. Not surprising for a technologist who's never been afraid to move to the beat of a different drum.

Or-Bach contributed pioneering ideas that helped establish the emerging category of structured ASICs. His concepts provided ways to reduce chip design costs from tens of millions to tens of thousands of dollars, while shortening design time from months to weeks.

In 1999, the conventional wisdom said standard-cell ASICs and FPGAs would crowd out gate arrays. Or-Bach had a different idea. In March of that year, he submitted a patent on a technique for blending an array of bit-stream programmable logic cells on a substrate with a mask-defined interconnection fabric overlay. That patent, issued in 2001—and 11 subsequent ones from Or-Bach's eASIC startup—paved the way for structured ASICs.

It all started back in 1982, when Or-Bach posited that someday engineers would have a new set of tools for pushbutton circuit design. Two years later, his concepts for realizing that vision became the basis for the Quick system and a new company, Chip Express Corp., which Or-Bach led for 10 years. Then his quest for an even better way to automate chip design led him to ideas for using direct electron-beam tools for commercial chip production, fueling the eASIC launch.

The serial entrepreneur now has 30 patents to his credit and plenty of energy left for the dance floor.

Serial entrepreneur sniffs out better ways to automate chip design.

Zvi Or-Bach

Erected the scaffolding for the structured ASIC